REMARKS

This Amendment responds to the Office Action mailed July 31, 2006 in the above-identified application. Based on the foregoing amendments and the following comments, reconsideration and allowance of the application are respectfully requested.

Claims 1, 4-6, 30, 32-33, 36, 39 and 41 are currently pending in the application. Claims 2-3, 7-29, 31, 34, 35, 37-38, 40 and 42-45 were previously cancelled. By this amendment, claims 1, 6, 30, 36 and 41 are amended. No new matter has been added.

The Examiner has rejected claims 1, 6, 30, 36, 39 and 41 under 35 U.S.C. § 103 as unpatentable over Sakai (U.S. 6,131,143) in view of Ebner et al. (U.S. 6,928,525). Claims 4-5 and 32-33 are rejected under 35 U.S.C. § 103(a) as unpatentable over Sakai in view of Ebner et al., and further in view of Liao et al. (U.S. 6,857,061). The rejections are respectfully traversed in view of the amended claims.

Sakai discloses a multi-way associative cache memory. The cache memory shown in Fig. 1 includes a decoder 1, first tag memory 2, second tag memories 3a, ... 3n, multi-way data memories 5a, ... 5n, comparators 6, 7a, ... 7n and way selector 9 (column 4, lines 25-28). Tag memory 2 stores high order bits of an address tag, and tag memories 3a, ... 3n store lower order bits of the address tag (column 4, lines 29-32). The high order address tag and the low order address tag of address 10 are compared with the contents of tag memories 2 and 3a, ... 3n by comparators 6 and 7a, ... 7n, respectively (column 4, line 36 to column 5, line 15). Sakai contains no disclosure or suggestion whatever of concurrent access to multi-way *data* memories 5a, ... 5n.

Ebner discloses a method for arbitrating a plurality of cache access requests to a cache memory having a plurality of cache lines and a plurality of access ports, including detecting requests to access the cache memory from a plurality of requestors, determining whether at least two of the plurality of requestors are seeking access to an identical one of the plurality of cache lines and allowing, if the at least two of the plurality of requestors are not seeking access to the

identical one of the plurality of cache lines, the plurality of requestors to concurrently access the cache memory through the plurality of access ports (column 2, lines 43-55). A cache arbiter allows concurrent access by a plurality of requestors to different cache lines (column 4, lines 37-46). Ebner contains no disclosure of a multi-way cache memory.

Sakai and Ebner, taken individually or in combination, do not disclose or suggest a cache memory wherein a first device accesses a data memory location, without limitation as to data memory location, in a first way and a second device concurrently accesses a data memory location, without limitation as to data memory location, in a second way. This operation is apparent from Fig. 3A of the present application, where decoders 206a-206d access different data memory locations independently and without being restricted by the operation of the other decoders. The decoders are blocked from accessing a way that is currently in use by a way enable register 504 shown in Fig. 5. Thus, decoders 206a-206d may concurrently access the same cache line in different ways of the cache memory. This operation is not taught or suggested by Sakai in view of Ebner.

Contrary to the assertion of the Examiner, Sakai does not disclose a controller that enables a first device to access a data memory location in a first way and enables a second device to access a data memory location in a second way. As described at column 5, lines 64-66 of Sakai, way selector 9 selects the data of the way for which a cache hit takes place and supplies the selected data to the data processing unit. Further, contrary to the assertion of the Examiner, Sakai does not disclose or suggest that the data memory locations in the first and second ways can be accessed concurrently by the first and second devices. The cited passage of Sakai at column 4, lines 37-46 describes operation of the *tag* memories to determine a cache hit rather than concurrent access to the multi-way data memories. In summary, Sakai contains no disclosure or suggestion of concurrent access to the multi-way data memories.

Ebner does not provide the teachings that are lacking in Sakai. Ebner describes a cache memory where a plurality of requestors can access different cache lines in the cache memory. However, Ebner contains no disclosure of a cache memory having two or more ways or how to

access such ways. Further, the Ebner cache memory does not permit concurrent access to the same cache line.

In summary, Sakai in view of Ebner do not disclose or suggest a cache memory wherein a first device is enabled to access a data memory location, without limitation as to data memory location, in a first way and a second device is enabled to concurrently access a data memory location, without limitation as to data memory location, in a second way, as required by Applicant's independent claims. For these reasons, independent claims 1, 6, 30, 36 and 41 are clearly and patentably distinguished over Sakai in view of Ebner.

Claims 4 and 5 depend from claim 1, claims 32 and 33 depend from claim 30 and claim 39 depends from claim 36. These claims are patentable over Sakai in view of Ebner for at least the same reasons as claims 1, 6, 30, 36 and 41.

Based upon the above discussion, claims 1, 4-6, 30, 32-33, 36, 39 and 41 are in condition for allowance.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

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